ABSTRACT OF THE DISCLOSURE

[1024] An improved power fail-safe has an effective maximum delay of two gate delays from an input operably powered by a first power supply to a first and a second output operably powered by a second power supply. The first and second outputs have predetermined values during an interval when the first power supply has failed and the second power supply is active. The first and second power supplies may be based at least in part on different power domains. The first power supply may be based at least in part on a core power domain and the second power supply may be based at least in part on an I/O power domain.